High Temperature Stack-chip, Die-attach Adhesive Developments

Currently solving many problems, but a new generation is needed.

By Kevin Chung, Ph.D. [AI Technology, Inc.]

The majority of die-attach applications for chip packaging are done with singulated dice and dispensed die-attach adhesive paste. Film adhesives have also been used for at least 10 years for stack-chip applications.

In recent years, the use of film die-attach adhesives in wafer-level packaging has been in high-volume use for DRAM applications with great success. In this type of thin wafer-level packaging where the resulting device size and thickness are critical to commercial success, die-attach film has been steadily reduced to 10μm or less in comparison to the 1-3mils bond line thickness for traditional die-attach semiconductor packages.

While electronic packages using die-attach adhesive can achieve substantial relief of the interfacial stresses with the use of thicker, low modulus adhesives, the use of epoxy film adhesive with a coefficient of thermal expansion (CTE) in the range of 40-60ppm/°C, modulus of more than 10 million PSI, and the bond-line thickness of 10-20μm have produced parts of adequate reliability for at least the DRAM packages.

In this paper, we will examine the criteria for wafer-level die attach with higher efficiency, more reliability and higher performance.

We will also examine the effects of interconnection from chip to package on the choice of die-attach solutions. The packaging, using wire bonding, flip-chip soldering, or the direct mechanical contact attach from flip-chip to bond pads, effectively dictates the choice of different wafer-level, die-attach solutions.

Wire bonding and flip-chip interconnections

Wire-bonding is the predominant choice for chip-to-package interconnections. The proven efficiency and reliability result in a cost effective solution for high volume DRAM applications.

Most of the stack-chip packaging for smaller volume production uses pre-cut, die-attach film with great success and high reliability. These earlier stack-chip solutions have been building DRAM with 8 or more chips for many high-end applications. These standard die-attach film adhesives tend to be a controlled thickness of 2-4mils. Figure 2 shows two examples of these 3-D high density packages.

As more chips are stacked on top of each other, wire-bonding interconnection becomes more difficult to execute. Many ingenious packaging schemes have been developed by, for example, Vertical Circuit Inc. on board flip-chip attach by Shellcase, and through-silicon via (TSV) from Sharp, Fujitsu, and others.

In high volume commercial applications, the use of 10-20μm die-attach film adhesive has proven to be reliable for this size and
shape of chip for stacked chips from two to three layers. With that number of stacked chips, wire bonding can still be managed. The use of 10-20μm film adhesive not only yields thinner devices that are attractive for cameras and other commercial applications, but also provide a more uniform and controlled flow of the adhesive and thus more reproducible wire-bonding interconnections.

Standard wire-bonding chip packaging uses backside die attach that can use more traditional epoxy die-attached film adhesives that are available from die-attach film adhesive manufacturers from the USA and Japan. Figure 3 shows a pre-laminated wafer with 15μm die-attach film adhesive.

Typical manufacturing process in using wafer-level packaging is now integrated in terms of using dicing tape and die-attach film that are directly laminated on the wafer before dicing. The layering of such configurations is illustrated in Figure 2 and the process represented in Figure 3.

Adhesive properties and device performance

The material technology challenges that enable the processes described in Figure 3 are many and have been met so far by dicing die-attach film (DDAF) adhesives that are available from die-attach film adhesive manufacturers from the USA and Japan. Most of the existing DDAF are meeting the performance requirements of JEDEC IPC level 3 or better for moisture sensitivity after packaging.

Depending on the bonding stability and moisture sensitive properties of DAF and the molding, encapsulation, or other electro-mechanical protection, the finished devices range from level 3 (in most cases) to the best solutions meeting the level 1 requirement.

In case of high temperature applications beyond 150°C, newer non-epoxy DAF can now withstand long-term usage of 200°C and beyond.

Die-bonding adhesive and stress relief protection

Traditional flip-chip uses wire bonding and solder-bump reflow for most requirements. Higher speed, performance, and cost continue to drive semiconductor packaging toward shorter path interconnections between each level of the stack-chip packages.

The need to lower the cost of packaging has led to many innovative packaging solutions. The lowest cost electronic devices such as UHF RFID tags have been successfully produced in large volume using direct flip-chip mechanical compression contact. However, they are limited to an operational temperature of less than 60°C and they are not very stable against moisture.

The fact that contact resistance can be properly maintained for long-term usage within specified temperature and environmental constraints provides hope that solutions for high performance applications can be achieved with more engineered materials and packaging. Figure 5 illustrates such flip-chip, direct contact interconnection.

The key for performance for this type of package is the flip-chip underfill that must also perform as a stable die-bonding adhesive. For the flip-chip underfill adhesive to function properly, it must possess at least the following characteristics:

1. Underfill adhesive must be easily placed either on the substrate or on the interconnection front side of the chip. Dicing die-attach film (DDAF) is still applicable. If paste underfill adhesive is to be useful,
it must stay in place after dispensing onto the substrate or chip.

2. The underfill adhesive must not prevent contact when the chip and package substrate interconnections are lined up and compressed for bonding. Unlike the use of Z-axis, uniaxial, conductive adhesive, any particulate could be detrimental to the achievement of interconnections.

3. High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.

4. The underfill adhesive should be as low in coefficient of thermal expansion (CTE) as that of higher filled traditional epoxy underfills (< 30 ppm/°C).

5. In order to provide reasonable productivity, the underfill adhesive must be capable of curing at 175-250°C in less than 10 seconds.

6. To meet the JEDEC IPC Level 1 moisture sensitivity requirements, the moisture absorption should be below 0.5% in saturation.

There are now non-epoxy based, high temperature, underfill adhesives in paste or film format in thickness of 25-75μm for such applications.

TSV, specialty underfill, and via filling for stress relief

TSVs stack-chip packaging represents the ultimate chip interconnection performance for stack-chip packages. The requirement for stress relief is even more critical to filling in the vias of the TSV structure and between the stacking chips.

For filling in the TSVs, the specialty fill-in adhesive requires the following characteristics:

- The fill-in adhesive must have extreme low viscosity to wick into the vias easily with the capillary forces.
- Once cured, they must have very low coefficient of expansion (CTE) and preferably substantially below 30ppm/°C.
- High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
- Fill-in adhesive should cure in less than 10 seconds at 175-250°C.

There are now non-epoxy based high temperature fill-in paste adhesives that can easily fill in vias of 20μm for such applications. Figure 6 depicts the TSV structure and the lamination between layers to provide stress relief.

Conclusions

Flip-chip electrical interconnection between a chip bumped with gold studs and its package substrate can be done by direct compression with high reliability and manufacturability. A new generation of flip-chip underfill adhesives are needed with low moisture absorption, high Tg, low CTE, and high modulus to provide the stress relief that enables even high I/O counts devices to be packaged with high reliability and low moisture sensitivity.

Similar flip-chip underfill adhesive can also be very effective for fill in of through silicon vias and provide stress relief between stacked chips.

References

12. 3D-TSVs spark packaging revolution; http://www.ectasia.com/STATIC/ARTICLE_IMAGES/200809/EEOL_2008SEP01_TPA_MFG_NT_01_VSfig1.jpg
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<td>≈ 12</td>
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<th>Company</th>
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<th>City, State, Zip</th>
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<th>Maximum Wafer Size (mm)</th>
<th>Bump Pitches (µm)</th>
<th>Bumping Services</th>
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<tr>
<td>International Micro Industries (IMI)</td>
<td>1951 Old Cuthbert Rd. Bldg 404</td>
<td>Cherry Hill, NJ 08034</td>
<td>~21</td>
<td>300</td>
<td>CM</td>
<td>Bumping and WLP utilizing electro deposition process and specializing in high aspect ratio, fine pitch and pillar bump technology</td>
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<td>EMS Tsukuba Factory 38-32 S-Chome, Minami-Cho Fuchu-Shi, Tokyo 183-0026, Japan</td>
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<td>~30</td>
<td>300</td>
<td>80µm (45µm diameter)</td>
<td>Ball placement, reflow, washing, inspection, quick delivery, low cost, high quality</td>
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<td>NEPES, Pte Ltd</td>
<td>12 Ang Mo Kio Street 65</td>
<td>Singapore 569060</td>
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<td>300</td>
<td>50 – 150</td>
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<td>Pac Tech GmbH</td>
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<td>Am Schlangenhorst 7-9 &amp; 15-17 14641 Nauen, Germany</td>
<td>~150</td>
<td>300</td>
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To update listings in the directory for next year’s publication, please contact the author at surveys@aztechdirect.com before January 31, 2011.
Nanoscale MEMS Made Inside a CMOS Wafer

A new technology to construct nanoscale MEMS within the structure of the actual CMOS wafer itself using standard, high volume CMOS lines, has been announced by Boalab Microsystems of Barcelona, Spain. The technology uses the existing metal layers in a CMOS wafer to form the MEMS structure using standard mask techniques. “We have solved the challenge of building MEMS in a completely different way,” explained Dave Doyle, Baolab’s CEO.

Baolab has successfully created MEMS devices using standard 0.18μm, 8” CMOS wafers with four or more metal layers, and has achieved minimum feature sizes down to 200 nanometres. The prototype stage has already proven the NanoEMS technology and evaluation samples will be available later this year. These are aimed at handset designers and manufacturers, and Power Amplifier and RF Front End Module markets. [www.baolab.com]

Gantry Robots Get More Capacity

DENSO, headquartered in Kariya, Japan, has announced that it has increased the payload capacity of its XR-Series four-axis, compact gantry robots from 3 kg to 5 kg. The new 5kg capacity, which represents an increase of over 60 percent, allows the robots to handle a significantly wider range of applications. The XR-Series robots feature a ceiling mounted, SCARA robot combined with a long-stroke Cartesian robot. They can operate in many applications without the need of a conveyor.

The robots have a reach of 200mm to 300mm, an x-axis stroke of 850mm to 1,660mm, a cycle time of 0.53 seconds, and repeatability of ±0.015mm. Typical applications include assembly, dispensing, material handling, and parts feeding. DENSO Robotics offer robots, controllers and software covering a wide range of applications. [www.densorobotics.com]

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The No. 836 is a 750°F, electrically-heated, Class 100 cleanroom oven from Grieve, Round Lake, IL, USA, and can be used to bake various coatings onto products at a customer’s facility. Workspace dimensions of this oven measure 36” wide x 36” deep x 39” high. Incoloy sheathed tubular heating elements provide 30KW of heating and a maximum temperature of 750°F. A 1000CFM, 1.5HP recirculating blower maintains horizontal airflow across the load. The oven has 6” insulated walls, a 2B finish stainless steel interior, and an aluminized exterior.

Additional equipment on this Grieve oven includes a 30” x 24” x 6” thick stainless steel high temperature HEPA recirculating air filter, digital programmable temperature controller, manual reset excess temperature controller with separate contactors, recirculating blower airflow safety switch, and a 10” diameter circular chart recorder. [www.grieveCorp.com]

New Test Socket Claims 500,000 Insertions

Ironwood Electronics of Burnsville, MN, USA, has recently introduced the new high performance socket for the 602PGA-SS-PGA27/602A-01. The contactor is a spring pin (pogo) with 27 grams actuation force per ball and cycle life of 500,000 insertions. The self-inductance of the contactor is 1.1nH with 50Ω matched impedance. The current capacity of each contactor is 5 amps. Socket temperature range is -55°C to +150°C. Kyocera’s PB602AUE63-1 and other PGA ICs that are 35x35mm body size, 1.27mm pitch, and 27x27 pin array can be tested. The Socket is constructed of aluminum which provides heat sinking up to several watts and custom heat sinks can easily be designed for higher power dissipation. This socket can be used for functional test and extreme thermal cycling test with the most stringent requirements. [www.ironwoodelectronics.com]

Bond Tester Has More Features

The Condor EZ, a new bond tester from XYZTEC, Gilroy, CA, USA, offers a single platform with multiple test capabilities. In addition to standard bond testing applications such as wire
pull, ball shear, and die shear, the Condor EZ has the capability to perform peel testing, push testing, and roller testing. All of these tests can be done on one test head that features four different measurement sensors. The system can perform mechanical shock testing by changing the test head for impact testing or ribbon peel testing of photovoltaic cells. All important software functions can be controlled by a single touch of a button to ensure simplicity. XYZTEC equipment is used worldwide throughout the semiconductor, automotive, solar and raw materials industries.

Incal Introduces ‘Inspire 8160 HX’ Power Burn-In System

Incal Technology, Inc. has just introduced its latest ‘Inspire 8160 HX’ System for the power device burn-in market.

The ‘Inspire 8160 HX’ System provides individual temperature control for low to medium power SOC and mixed signal devices up to 60 Watts. It uses thermal sockets and the well established Incal XP-160 driver and Inspire system software.

As thermal control and management is at the DUT level, no conventional thermal chamber is required. Since XP-160 /Inspire continue to be the main system architecture, all currently available burn-in system capabilities (drive and monitoring) and features are available for this ‘NEW’ system, including the ‘Analog Option’. This ‘Inspire 8160 HX’ System addresses the increasing concern of power dissipation of high-power semiconductor devices. The power consumed by high-power semiconductor devices can vary by up to 50%, due to variation in fabrication process.

This causes a large variation in temperature among the same devices in the burn-in chamber. In order to burn-in all devices at the same junction temperature, there is a need for Individual ‘Temperature Control’ per DUT. This ‘Inspire 8160 HX’ System provides individual temperature control at the DUT. Two major Independent Test Laboratories have purchased this ‘system’, adding this to many Incal standard HTOL Infinity/Inspire systems on their floor.
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7. ☐ Semiconductor Test
8. ☐ Semiconductor Materials
9. ☐ Military/Government
10. ☐ Industrial/Medical/Automotive
11. ☐ University or Research Organization
12. ☐ Other (please describe) ______________________________________

C

Please indicate your primary job function. (check only one)

13. ☐ Assembly/Package Engineering
14. ☐ Corporate or General Management
15. ☐ Test Engineering
16. ☐ Engineering Management
17. ☐ IC Design Engineering
18. ☐ Manufacturing Management
19. ☐ PC Board Design or Fabrication
20. ☐ Purchasing
21. ☐ R&D
22. ☐ Sales and Marketing
23. ☐ Consultant
24. ☐ Other (please describe)

D

What products do you buy or specify?

PRODUCTION EQUIPMENT

25. ☐ Assembly Equipment/Materials for ICs
26. ☐ Semiconductor Packaging Foundry Services
27. ☐ Other Components
28. ☐ Design or Fabrication Services
29. ☐ Test Equipment
30. ☐ Inspection Equipment
31. ☐ Encapsulation Equipment, Materials
32. ☐ Wire or Die Bonders
33. ☐ Sockets/Handlers
34. ☐ Wafer Bumping/Probing
35. ☐ Substrates

MATERIALS

36. ☐ Adhesives/Solder
37. ☐ Cleaning Solutions/Materials
38. ☐ Other (please describe)

39. ☐ None of the above

E

What other publications are currently personally addressed to you?

(Check all that apply.)

40a. ☐ Solid State Technology/Advanced Packaging (digital)
40b. ☐ Solid State Technology/Advanced Packaging (print)
41a. ☐ Circuits Assembly (digital)
41b. ☐ Circuits Assembly (print)
42. ☐ Global SMT Packaging
43. ☐ MEPTEC Report
44a. ☐ Semiconductor International (digital)
44b. ☐ Semiconductor International (print)
45a. ☐ SMT (digital)
45b. ☐ SMT (print)
46c. ☐ SMT/Hybrid

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