

High Temperature Stack-chip, Die-attach Adhesive Developments

Currently solving many problems, but a new generation is needed.

By Kevin Chung, Ph.D. [AI Technology, Inc.]

The majority of die-attach applications for chip packaging are done with singulated dice and dispensed die-attach adhesive paste. Film adhesives have also been used for at least 10 years for stack-chip applications.

In recent years, the use of film die-attach adhesives in wafer-level packaging has been in high-volume use for DRAM applications with great success. In this type of thin wafer-level packaging where the resulting device size and thickness are critical to commercial success, die-attach film has been steadily reduced to 10 μ m or less in comparison to the 1-3mils bond line thickness for traditional die-attach semiconductor packages.



Figure 1. CPU is one of the great successes of flip-chip application

DRAM is usually rectangular with a total overall die-attach area smaller than one square centimeter. This enables the use of thin bond lines of less than 10 μ m without excessive internal stress-induced failures even when the bond is reduced to much less than the commonly acceptable bond line of 1.5-3mils for reliable die-attach thickness¹.

While electronic packages using die-attach adhesive can achieve substantial relief of the interfacial stresses with the use of thicker, low modulus

adhesives^{2,3}, the use of epoxy film adhesive with a coefficient of thermal expansion (CTE) in the range of 40-60ppm/ $^{\circ}$ C, modulus of more than 10 million PSI, and the bond-line thickness of 10-20 μ m have produced parts of adequate reliability for at least the DRAM packages.

In this paper, we will examine the criteria for wafer-level die attach with higher efficiency, more reliability and higher performance.

We will also examine the effects of interconnection from chip to package on the choice of die-attach solutions. The packaging, using wire bonding, flip-chip soldering, or the direct mechanical contact attach from flip-chip to bond pads, effectively dictates the choice of different wafer-level, die-attach solutions.

Wire bonding and flip-chip interconnections

Wire-bonding is the predominant choice for chip-to-package interconnections. The proven efficiency and reliability result in a cost effective solution for high volume DRAM applications.

Most of the stack-chip packaging for smaller volume production uses pre-cut, die-attach film with great success and high reliability. These earlier stack-chip solutions have been building DRAM with 8 or more chips for many high-end applications. These standard die-attach



Figure 2. Stack-chip packages can be interconnected with wire bonding or special design inter-chip interconnection bridges

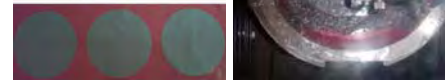
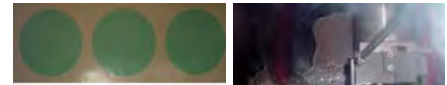


Figure 3a. Lamination of wafer onto dicing die-attach film (DDAF)

Figure 3b. Dicing wafer with DDAF



Figure 3c. Shining UV to release dice



Figure 3d. Pickup dice from DDAF



Figure 3e. Examining dice for packaging

film adhesives tend to be a controlled thickness of 2-4mils. **Figure 2** shows two examples of these 3-D high density packages.

As more chips are stacked on top of each other, wire-bonding interconnection becomes more difficult to execute. Many ingenious packaging schemes have been developed by, for example, Vertical Circuit Inc.⁴, on board flip-chip attach by Shellcase, and through-silicon via (TSV) from Sharp, Fujitsu, and others⁵.

In high volume commercial applications, the use of 10-20 μ m die-attach film adhesive has proven to be reliable for this size and

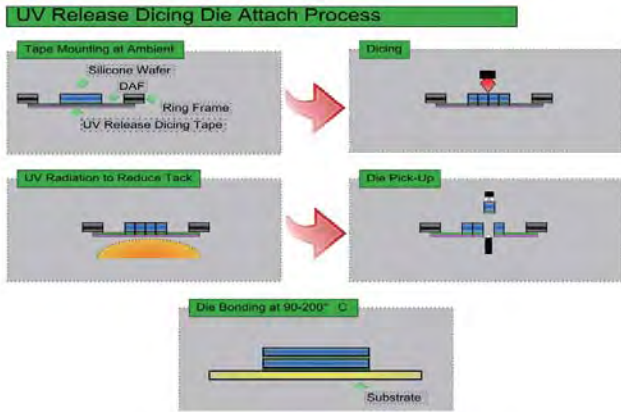


Figure 3. Dicing die-attach film processing. Die-attach film must be compatible with UV release layer and have the ability to flow and cure rapidly, or flow with light pressure and cure without pressure, in order to maintain productivity

shape of chip for stacked chips from two to three layers. With that number of stacked chips, wire bonding can still be managed. The use of 10-20µm film adhesive not only yields thinner devices that are attractive for cameras and other commercial applications, but also provide a more uniform and controlled flow of the adhesive and thus more reproducible wire-bonding interconnections.

Standard wire-bonding chip packaging uses backside die attach that can use more traditional epoxy die-attached film adhesives that are available from die-attach film adhesive manufacturers from the USA^{6,7} and Japan^{8,9,10}. Figure 3 shows a pre-laminated wafer with 15µm die-attach film adhesive.

Typical manufacturing process in using wafer-level packaging is now integrated in terms of using dicing tape and die-attach film that are directly laminated on the wafer before dicing. The layering of such configurations is illustrated in Figure 2 and the process represented in Figure 3.

Adhesive properties and device performance

The material technology challenges that enable the processes described in Figure 3 are many and have been met so far by dicing die-attach film (DDAF) adhesives from the USA and Japan. The following are some of the challenges:

- Very thin and stable film adhesive (typically epoxy-based) of 10-25µm

for the largest wafer today (12 inches).

- DAF film adhesive must be compatible with the use of UV release dicing tape to release chip after dicing operations.
- Ability to allow stack-chip bonding with high efficiency.
- Ability to provide die-bonding stability for wire-bonding operation of up to 250°C for the highest production rate possible.

- Most of the existing DDAF are meeting the performance requirements of JEDEC IPC level 3 or better for moisture sensitivity after packaging.
- Depending on the bonding stability and moisture sensitive properties of DAF and the molding, encapsulation, or other electro-mechanical protection, the finished devices range from level 3 (in most cases) to the best solutions meeting the level 1 requirement.
- In case of high temperature applications beyond 150°C, newer non-epoxy DAF can now withstand long-term usage of 200°C and beyond.

Die-bonding adhesive and stress relief protection

Traditional flip-chip uses wire bonding and solder-bump reflow for most requirements. Higher speed,

performance, and cost continue to drive semiconductor packaging toward shorter path interconnections between each level of the stack-chip packages.

The need to lower the cost of packaging has led to many innovative packaging solutions. The lowest cost electronic devices such as UHF RFID tags have been successfully produced in large volume using direct flip-chip mechanical compression contact¹¹. However, they are limited to an operational temperature of less than 60°C and they are not very stable against moisture.

The fact that contact resistance can be properly maintained for long-term usage within specified temperature and environmental constraints provides hope that solutions for high performance applications can be achieved with more engineered materials and packaging. Figure 5 illustrates such flip-chip, direct contact interconnection.

The key for performance for this type of package is the flip-chip underfill that must also perform as a stable die-bonding adhesive. For the flip-chip underfill adhesive to function properly, it must possess at least the following characteristics:

1. Underfill adhesive must be easily placed either on the substrate or on the interconnection front side of the chip. Dicing die-attach film (DDAF) is still applicable. If paste underfill adhesive is to be useful,

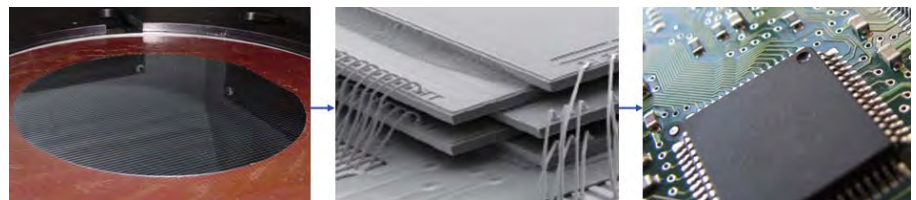


Figure 4. Semi-conductor packaging from wafer DDAF to component



Figure 5. Flip-chip interconnection with direct mechanical contacts between precious metal bumps and preservations on chip and package substrate respectively

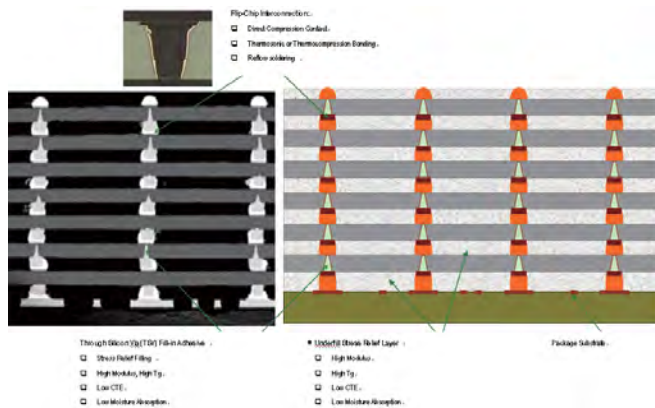


Figure 6. Specialty fill-in adhesive and underfill adhesive with low CTE, high modulus and high Tg is essential in the reliability of stack-chip packages using through TSV technology

it must stay in place after dispensing onto the substrate or chip.

- The underfill adhesive must not prevent contact when the chip and package substrate interconnections are lined up and compressed for bonding. Unlike the use of Z-axis, uniaxial, conductive adhesive, any particulate could be detrimental to the achievement of interconnections.
- High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
- The underfill adhesive should be as low in coefficient of thermal expansion (CTE) as that of higher filled traditional epoxy underfills (< 30 ppm/°C).
- In order to provide reasonable productivity, the underfill adhesive must be capable of curing at 175-250°C in less than 10 seconds.
- To meet the JEDEC IPC Level 1 moisture sensitivity requirements, the moisture absorption should be well below 0.5% in saturation.

There are now non-epoxy based, high temperature, underfill adhesives in paste or film format in thickness of 25-75µm for such applications.

TSV, specialty underfill, and via filling for stress relief

TSV¹² stack-chip packaging represents the ultimate chip interconnection performance for stack-chip packages. The requirement for

stress relief is even more critical to filling in the vias of the TSV structure and between the stacking chips.

For filling in the TSVs, the specialty fill-in adhesive requires the following characteristics:

- The fill-in adhesive must have extreme low viscosity to wick into the vias easily with the capillary forces.

- Once cured, they must have very low coefficient of expansion (CTE) and preferably substantially below 30ppm/°C.
- High glass transition temperature and modulus are required to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
- Fill-in adhesive should cure in less than 10 seconds at 175-250°C.

There are now non-epoxy based high temperature fill-in paste adhesives that can easily fill in vias of 20µm for such applications. **Figure 6** depicts the TSV structure and the lamination between layers to provide stress relief.

Conclusions

Flip-chip electrical interconnection between a chip bumped with gold studs and its package substrate can be done by direct compression contact with high reliability and manufacturability. A new generation of flip-chip underfill adhesives are needed with low moisture absorption, high Tg, low CTE, and high modulus to provide the stress relief that enables even high I/O counts devices to be packaged with high reliability and low moisture sensitivity.

Similar flip-chip underfill adhesive can also be very effective for fill in of through silicon vias and provide stress relief between stacked chips.

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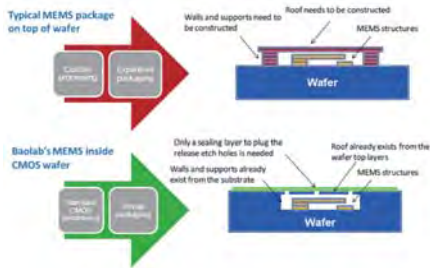
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WHAT'S NEW!

Nanoscale MEMS Made Inside a CMOS Wafer

A new technology to construct nanoscale MEMS within the structure of the actual CMOS wafer itself using standard, high volume CMOS lines, has been announced by Baolab Microsystems of Barcelona, Spain. The technology uses the existing metal layers in a CMOS wafer to form the MEMS structure using standard mask techniques. "We have solved the challenge of building MEMS in a completely different way," explained Dave Doyle, Baolab's CEO.



Baolab has successfully created MEMS devices using standard 0.18 μ m, 8" CMOS wafers with four or more metal layers, and has achieved minimum feature sizes down to 200 nanometres. The prototype stage has already proven the NanoEMS technology and evaluation samples will be available later this year. These are aimed at handset designers and manufacturers, and Power Amplifier and RF Front End Module markets. [www.baolab.com]

Gantry Robots Get More Capacity

DENSO, headquartered in Kariya, Japan, has announced that it has increased the payload capacity of its XR-Series four-axis, compact gantry robots from 3 kg to 5 kg. The new 5kg capacity, which represents an increase of over 60 percent, allows the robots to handle a significantly wider range of applications. The XR-Series robots feature a ceiling mounted, SCARA robot combined with a long-stroke Cartesian robot. They can operate in many applications without the need of a conveyor.



The robots have a reach of 200mm to 300mm, an x-axis stroke of 850mm to 1,660mm, a cycle time of 0.53 seconds, and repeatability of ± 0.015 mm. Typical applications include assembly, dispensing, material handling, and parts feeding. DENSO Robotics offer robots, controllers and software covering a wide range of applications. [www.densorobotics.com]

Need a Class 100 Oven?

The No. 836 is a 750°F, electrically-heated, Class 100 cleanroom oven from Grieve, Round Lake, IL, USA, and can be used to bake various coatings onto products at a customer's facility. Workspace dimensions of this oven measure 36" wide x 36" deep x 39" high. Incoloy sheathed tubular heating elements provide 30KW of heating and a maximum temperature of 750°F. A 1000CFM, 1.5HP recirculating blower maintains horizontal airflow across the load. The oven has 6" insulated walls, a 2B finish stainless steel interior, and an aluminized exterior.



Additional equipment on this Grieve oven include a 30" x 24" x 6" thick stainless steel high temperature HEPA recirculating air filter, digital programming temperature controller, manual reset excess temperature controller with separate contactors, recirculating blower airflow safety

switch, and a 10" diameter circular chart recorder. [www.grievcorp.com]

New Test Socket Claims 500,000 Insertions

Ironwood Electronics of Burnsville, MN, USA, has recently introduced the new high performance socket for the 602PGA-SS-PGA27/602A-01. The contactor is a spring pin (pogo) with 27 grams actuation force per ball and



cycle life of 500,000 insertions. The self-inductance of the contactor is 1.1nH with 50 Ω matched impedance. The current capacity of each contactor is 5 amps. Socket temperature range is -55°C to +150°C. Kyocera's PB602AUE63-1 and other PGA ICs that are 35x35mm body size, 1.27mm pitch, and 27x27 pin array can be tested. The Socket is constructed of aluminum which provides heat sinking up to several watts and custom heat sinks can easily be designed for higher power dissipation. This socket can be used for functional test and extreme thermal cycling test with the most stringent requirements. [www.ironwoodelectronics.com]

Bond Tester Has More Features

The Condor EZ, a new bond tester from XYZTEC, Gilroy, CA, USA, offers a single platform with multiple test capabilities. In addition to standard bond testing applications such as wire



pull, ball shear, and die shear, the Condor EZ has the capability to perform peel testing, push testing, and roller testing. All of these tests can be done on one test head that features

four different measurement sensors. The system can perform mechanical shock testing by changing the test head for impact testing or ribbon peel testing of photovoltaic cells. All

important software functions can be controlled by a single touch of a button to ensure simplicity. XYZTEC equipment is used worldwide throughout the semiconductor, automotive, solar and raw materials industries. [www.xyztec.com]

Incal Introduces 'Inspire 8160 HX' Power Burn-In System

Incal Technology, Inc. has just introduced its latest 'Inspire 8160 HX' System for the power device burn-in market.

The 'Inspire 8160 HX' System provides individual temperature control for low to medium power SOC and mixed signal devices up to 60Watts. It uses thermal sockets and the well established Incal XP-160 driver and Inspire system software.

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This causes a large variation in temperature among the same devices in the burn-in chamber. In order to burn-in all devices at the same junction temperature, there is a need for Individual 'Temperature Control' per DUT. This 'Inspire 8160 HX' system provides individual temperature control at the DUT. Two major Independent Test Laboratories have purchased this 'system', adding this to many Incal standard HTOL Infinity/Inspire systems on their floor.

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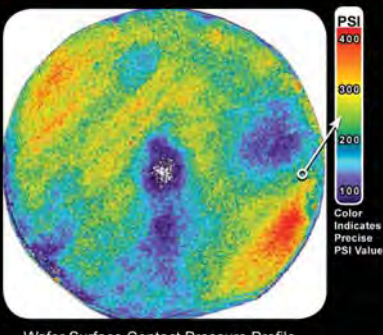


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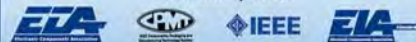
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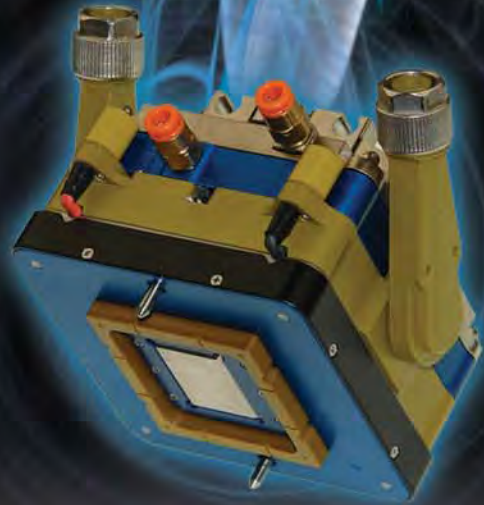
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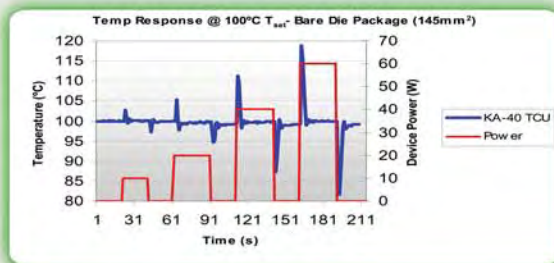
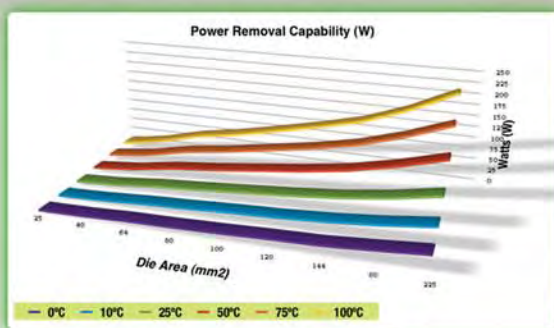
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